

FIG. 1

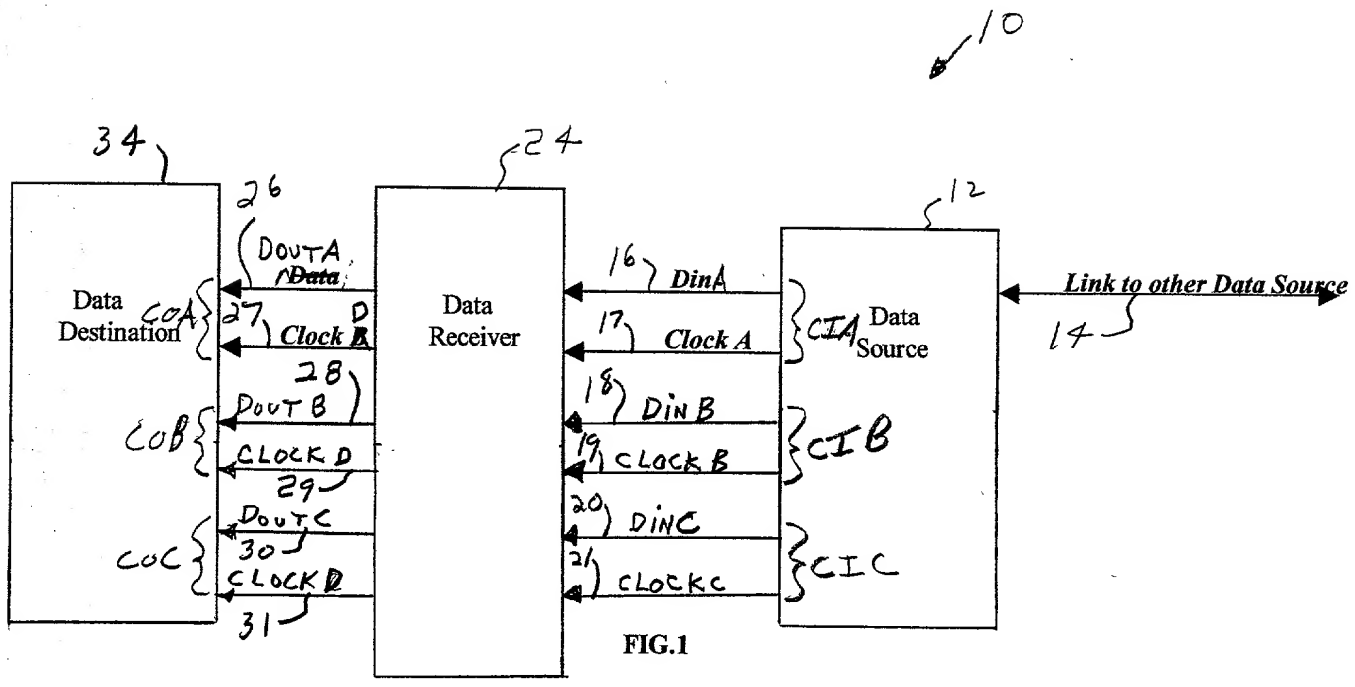


FIG.1

Clock A
Clock B

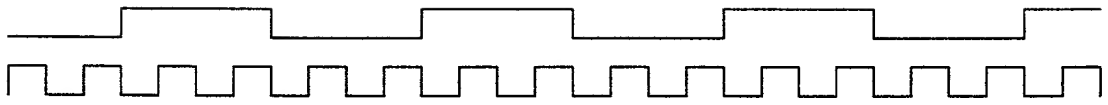


FIG. 2

Clock A
Clock B

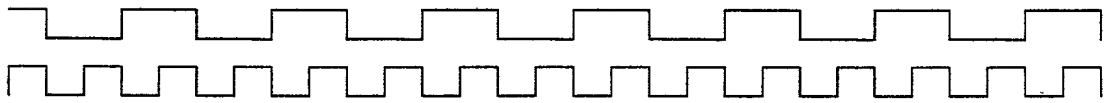


FIG. 3

Clock A
Clock B

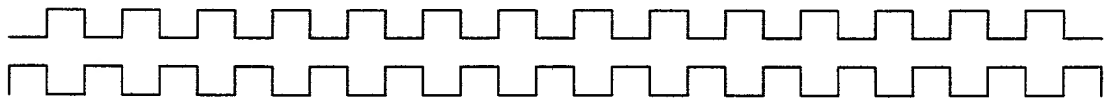
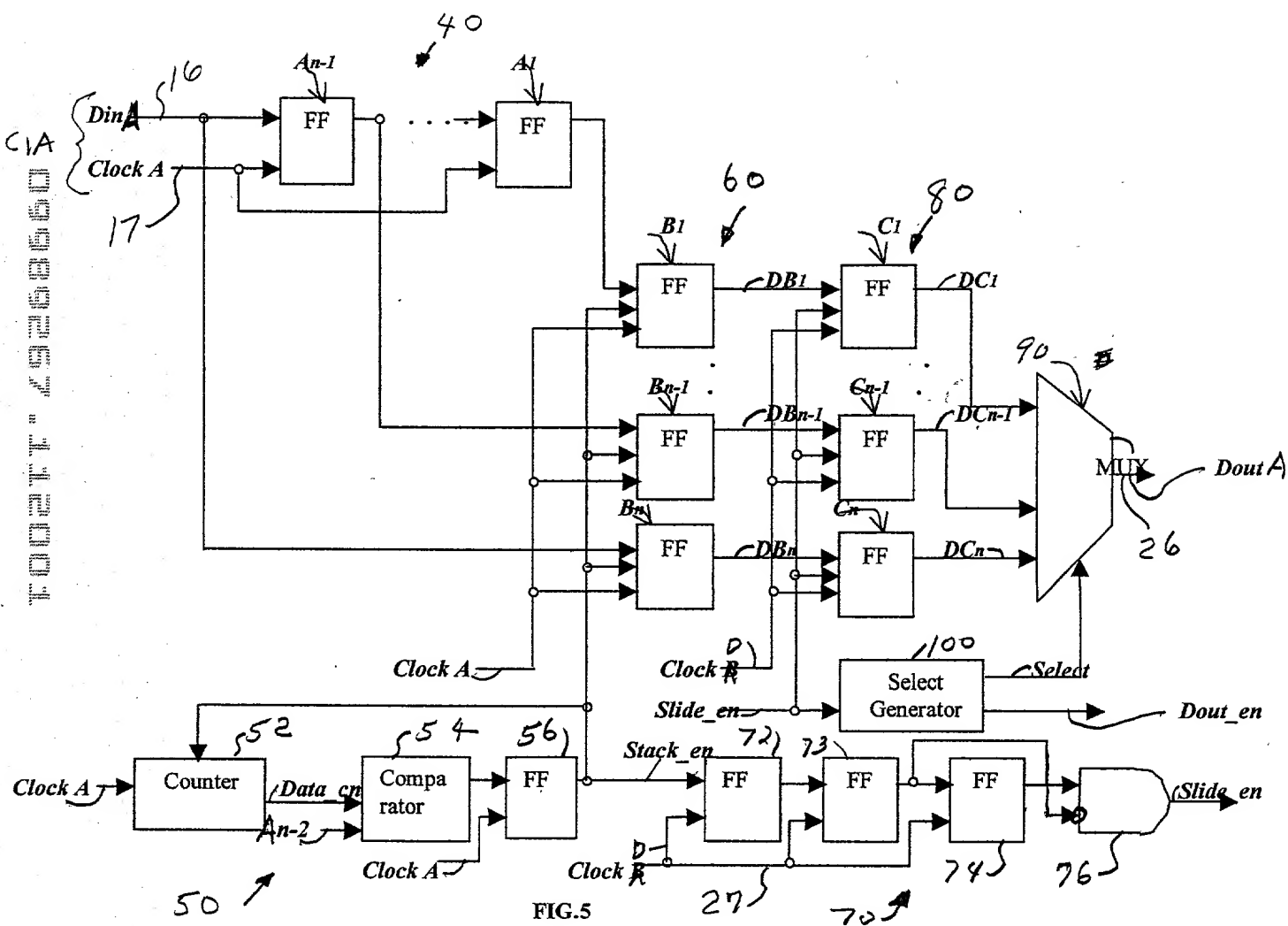


FIG. 4

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The timing diagram shows the following signals and their behavior:

- Din**: A sequence of data words D2, D3, D4, and D5.
- Clock A**: A periodic clock signal.
- Stack_en**: An enable signal that transitions from 100 to 101 at the start of the D3 word.
- DB3**: Data bus 3, which carries D3.
- DB2**: Data bus 2, which carries D2.
- DB1**: Data bus 1, which carries D1.
- Slide_en**: An enable signal that transitions from 102 to 103 at the start of the D3 word.
- DC3**: Data bus 3, which carries D3.
- DC2**: Data bus 2, which carries D2.
- DC1**: Data bus 1, which carries D1.
- Dout**: A sequence of data words D1, D2, and D3.
- Dout_en**: An enable signal that transitions from 103 to 104 at the start of the D3 word.
- Clock B**: A periodic clock signal.

FIG.6